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An Alternate Approach for Domestic Power Saver

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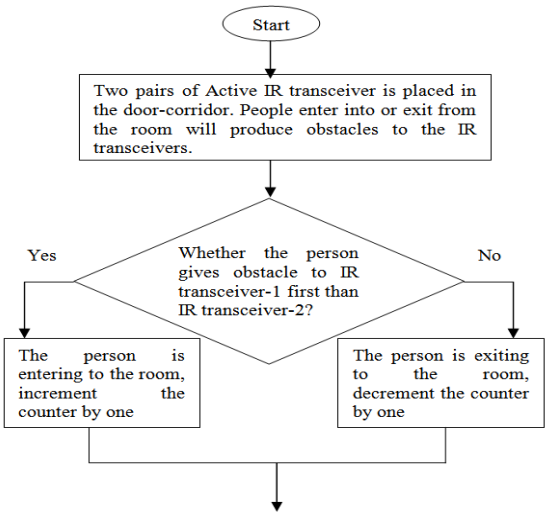
Abstract—*The amount of usage of electric power in domestic purpose have been significantly increased as users forget to switch off the lights and fans while they are going out of the room. An approach of user counting algorithm is documented here in this manuscript in order to automatically turn off lights and fans to prevent unnecessary wastage of electric power. A binary counter will be incorporated in order to take care of total count of person currently present in the room. Infra-Red signal is used to track the entrance and exit of a person through the corridor in front of a door in order to increase or decrease the people count of the room and subsequently turn off the load whenever the count reduced to zero by using an electromagnetic relay arrangement.*

1. INTRODUCTION

The domestic usage of electricity has been significantly increased during these recent years. The 24x7 use of electric lights and fans are common feature in modern cities. The usage of electricity in domestic purpose may add to extra electrical power consumption due to the forgetfulness of users who keep their lights and fans turning on even after they leave the room. This manuscript proposes an alternate and cheap solution to this problem and this system will count the number of persons inside the room and subsequently turn off the lights and fans whenever the count is decremented to zero. The algorithm is shown in the form of flowchart below.



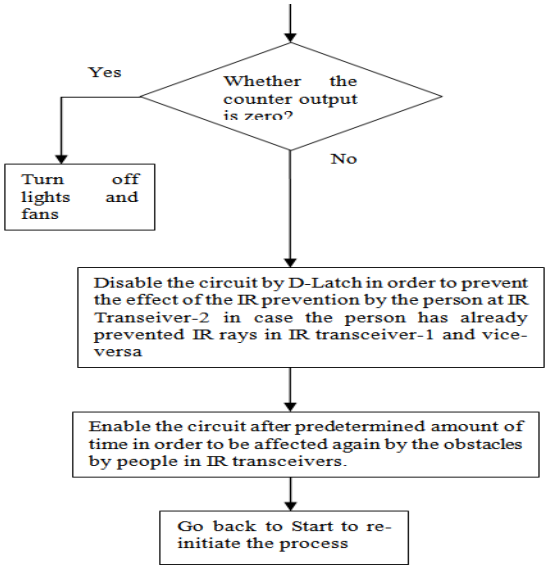


Fig. 1: Flowchart of the proposed algorithm.

The two pair of IR transceiver will serve as indicating device of whether the person is entering or exiting from the room. If transceiver-1, which is placed closer to the door, gets obstacle first by user, the up counter will be initiated and the circuit will be immediately gets latched by D-Latch IC.

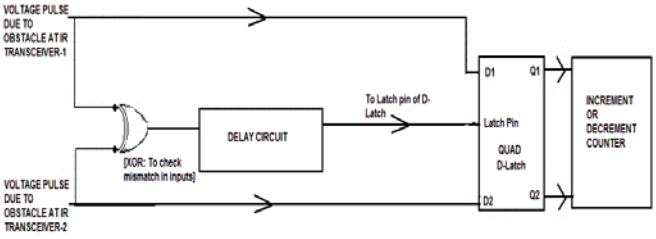


Fig. 2: Block Diagram of the proposed circuit.

The latching prevents the effects of the obstacle to IR transceiver-2, which is placed away from the door. If a person is exiting from the room, he will generate obstacle to IR

transceiver-2 before IR-tranceiver-1. In this case, the down counter will be initiated and after one step down counting, the circuit will again be latched in order to nullify the effect of IR-transceiver-1 to the system. The block diagram of the circuit is given below in Fig. 2.

The delay circuit shown in Fig. 2 is used to allow the counter circuit to be incremented or decremented by once after that the latch input of Quad D-Latch IC will become active and no further inputs from any IR Transceiver can affect the circuit. It ensures whenever voltage pulse from IR Transceiver-1 comes to increase the counter as person obstacles through the ray path between IR transmitter-1 and receiver-1, it will subsequently block any voltage pulse from IR Transceiver-2 to affect the counter circuit when the same person will block the ray path between IR transmitter-2 and IR-receiver-2 after some seconds.

2. IMPLEMENTATION OF DELAY CIRCUIT

The internal circuit diagram of delay circuit is shown in Fig. 3 below.

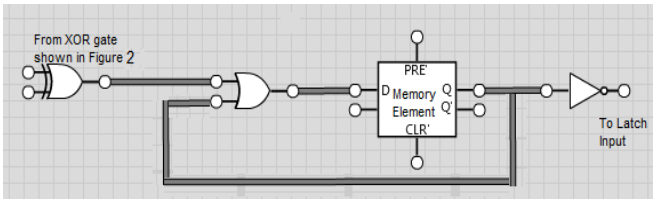


Fig. 3: Circuit Diagram of Delay circuit.

The delay circuit is implemented by one bit storage element (preferably by D flip-flop) and a feedback path from the flip-flop. If any of the XOR input goes to high due to voltage pulse from one of IR transceiver, it will set the D flip-flop and the output of D flip-flop will retain its value through the OR gate at the D input and thus a low pulse will always flow to the latch input of Quad D-Latch IC through an inverter after D flip-flop. The active low latch input of Quad D-Latch will become latched after the propagation delay through the gates and the D flip-flop propagation delay. This will ensure first IR transceiver voltage pulse from either IR-transceiver-1 or IR-transceiver-2 will affect the counter and voltage pulses from subsequent IR transceiver will be unable to affect the counter circuit in order to ensure only one time increment and decrement of counter value for one person.

3. QUAD D-LATCH

IC 74LS75 is a Quad D-Lach IC which consists four separate D-Latch (D1-Q1, D2-Q2, D3-Q3, D4-Q4). The D1-Q1 and D2-Q2 latches are used to get inputs from IR-transceiver-1 and IR-transceiver-2 respectively. The latch input is an active low input which latches the corresponding D-Latch when Latch input goes low. The truth table and the functionality of Latch input is shown in Table 1 below.

Table 1: Functionality of Latch Input of D-Latch.

D	Latch Input	Output
0	1	0
1	1	1
X	0	Previous Output

From Table 1, it can be found that in order to ensure the circuit should not be affected by IR transceiver voltage inputs, the high output of the delay circuit should go through inverter circuit. After latching, the output will always retain its previous value irrespective of the IR transceiver inputs. This will ensure only one increment or decrement of counter for one entrance or exit of a person.

After one complete entrance or exit of a person, the latched circuit should be made transparent to new inputs. A delay unit has been established to ensure the circuit will get transparent to new IR transceiver inputs. This delay time is currently set for five seconds after that the circuit will become active.

The delay time interval for the reactivation process is kept more than the delay unit shown in Fig. 2. The incorporation of this delay circuit is shown in Fig. 4.

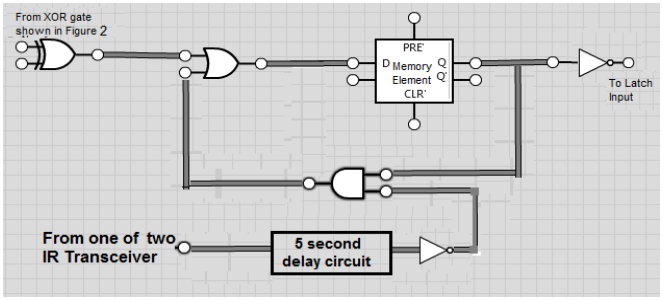


Fig. 4: 5 Second Interval Reactivation Delay Circuit Implementation.

Initially the output of the 5 second delay circuit is low which generates a high output from inverter. This voltage and another high output from D flip-flop will make the output of AND gate high. This will regenerate high input to the D input of D flip-flop. Thus a low input will be always fed to the Latch input and the system remains latched or disabled, non-responsive to any IR transceiver inputs. Once a high pulse from any IR transceiver comes to the input of the 5 second delay circuit, a high pulse goes to the input of the next inverter circuit which in consequence generates a low output for a brief period. This low output will generate low output from the AND gate connected at the output of the inverter. Now a low pulse will come to the input of D flip-flop and it in response, generates a low output. The low output is inverted and fed to Latch input

of Quad D-Latch. The high input at Latch input makes all the D-Latches transparent to the new inputs from IR transceivers. In this process, the circuit can be reactivated for the new count.

4. COUNTER AND ELECTROMAGNETIC RELAY CIRCUIT

The same digital counter is used for up counting and down counting. The square wave oscillator output is ANDed with the Q1 and Q2 output from D-Latch IC. Depending on whether Q1 or Q2 is on, the count gets increased or decreased. The output of the counter is fed to an electromagnetic relay through a decoder and proper current amplification stages. The current amplification is necessary in order to provide rated current to electromagnetic relay to energize it. A common-emitter mode transistor is used to increase the output current than the input at base. The circuit connection from digital counter to electromagnetic relay is shown in Fig. 5.

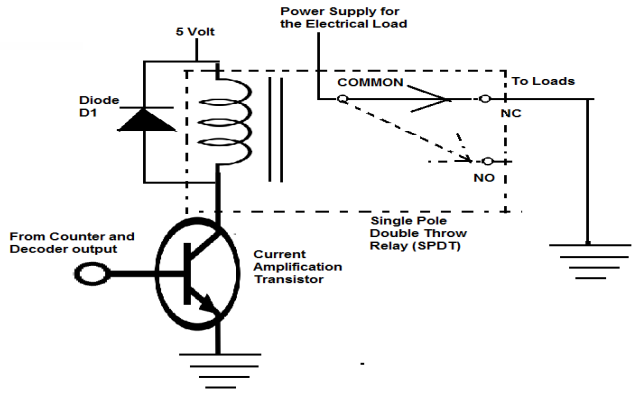


Fig. 5: Electromagnetic SPDT Relay Connection and Suitable Current Amplification.

The objective is to turn off loads whenever the counter output goes to zero. This is accomplished by a Single Pole Double Throw Electromagnetic Relay (SPDT). The power supply path to a specific load is situated alongside the connection between 'Common' and 'Normally Connected (NC)'. Whenever relay gets excited, the connection between 'Common; and NC is disconnected and 'common' gets connected to 'Normally Open (NO)'. Thus the power supply to that load is tripped. This methodology can be implemented to any loads in the room. To get proper exciting current to relay, a current amplification stage is designed with a common emitter mode npn transistor. A power diode (D1) is attached to the circuit in order to protect the transistor from the back emf when the relay is turned off. In this process, a cheap and easily implementable approach can be implemented in order to save unnecessary power wastage by turning the domestic loads off automatically when it is not used.

5. CIRCUIT IMPLEMENTATION PROGRESS

Currently the circuit up to the binary counter has been designed and tested. The relay circuit is also tested and about to be connected to the main circuit.

6. ADVANTAGE OF THIS APPROACH

The following advantages can be summarized for this implementation.

1. This approach is very cheap and very easy to incorporate in domestic purpose.
2. This circuit can be implemented to any domestic
3. Loads as well as industrial loads.
4. This circuit can also be utilized to turn on the corresponding load by simply interchanging the NO and NC connections. This will help any disabled persons to turn on lights and fans automatically.
5. This system will save electrical power from being wasted due to the forgetfulness of users.

7. ACKNOWLEDGEMENTS

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